R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a first clock signal and (ii) two or more serial data signals. The second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102 as being anticipated by Mullaney et al. '575 is respectfully traversed and should be withdrawn.

Mullaney discloses a high speed cross point switch routing circuit with a word-synchronous serial back plane (Title).

In contrast, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) two or more serial data signals. A second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

The so-called first circuit (elements 60, 86 and 98 in FIG. 6 of Mullaney) does not appear to present two or more serial data signals to the so-called second circuit (elements 58, 62 and 94 of Mullaney), as presently claimed. In particular, the input to the circuit 86 does not appear to receive two or more serial data signals, as presently claimed. The output of the circuit 94 does not appear to present two or more serial data signals, as presently claimed. FIG. 5b of Mullaney clearly only shows one input to the circuit 86 and one output from the circuit 94. Therefore, Mullaney does not disclose or suggest each of the elements of the present claims. As such, the presently pending claims are fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the amendment to claims 1, 9 and 10 does not raise new issues since claims 17-20 (previously pending) provide that the first circuit responds to a plurality of serial data signals and the second circuit presents the plurality of serial data signals. The explanation that the serial to parallel converter 60 receives one serial signal after another, does not appear to be relevant, since one serial signal after another is still only one serial signal.

In conclusion, Mullaney does not disclose or suggest a second circuit configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal. As such, the

presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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